

Docket No.: 1614.1383

Serial No. 10/773,232

**IN THE SPECIFICATION:**

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

MLB 10/9/06

Please REPLACE the paragraph beginning at page 1, line <sup>19</sup>26, with the following paragraph:

A so-called read register circuit is a register from which a CPU can read out predetermined information provided in a peripheral circuit of a so-called UART (universal asynchronous receiver-transmitter) ~~or so~~. A specific example thereof is a circuit which provides a DCTS (delta clear to send) bit for an MSR (modem status register) providing an I/O port of a well-known 16450/16550 ~~type type~~ UART.

Please REPLACE the paragraph beginning at page 9, line 4, with the following paragraph:

The above-mentioned examples are so-called level-detecting-type read clear DCTS bit circuits having a configuration in which a status detection signal is input to an asynchronous reset input terminal of a FF (flip-flop) device or a latch device. Therefore, in case the active interval of the status detection signal is longer than the active interval of the register reading out signal, there is a possibility that the status is read out twice or more even with ~~once~~ only one occurrence of the detection signal. If such a phenomenon occurs, a CPU which reads out the status may malfunction, and as a result, the whole system around the CPU may be damaged. Such a situation in which the active interval of the status detection signal is longer than the active interval of the register reading out signal may occur as the period of the register reading out signal is reduced as a result of increase in the system operation speed, i.e., the operation clock rate. A condition of occurrence of such a problem will now be discussed in detail.